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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/421,437	10/19/99	CHAPMAN	D 50265-018

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EXAMINER	
THOMPSON, A	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 02/09/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/421,437	David C. CHAPMAN
Examiner	**Group Art Unit**
A.M. Thompson	2825

☒ Responsive to communication(s) filed on *Nov 20, 2000*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-34* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-34* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Oct 19, 1999* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Applicant's Amendment and Response to application, serial number 09/421,437, has been examined and reviewed. Claim 34 is added. Claims 1, 3, 10, 18, 22, 24, 26, 29, and 31 are amended. Claims 1-34 are pending.

1. This second action on the merits cites new grounds for rejection and prior art that more persuasively reads on Applicant's claim limitations. Accordingly, this second action effectively moots Applicant's response to the first office action, Paper No. 5.

Drawings

2. Figures 1A, 1B, 2, and 3A, 3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defects can be deferred until the application is allowed by the examiner.

Claim Objections

4. Claims ok 24 and ok 29 are objected to because of the following informalities: Pursuant to Claim 24, at lines 5, 7, 15, and 19, the gerund (-ing) form of the verb should be used. Pursuant to Claim 29, at lines 10, 16, and 21, the gerund (-ing) form of the verb should be used. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Pursuant to Claim 12, at line 5, "routing the routing path" is unclear. Examiner suggests *routing the path.*

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claims 1-6, 10-20, 22, 24-34

8. **Claims 1-6, 10-20, 22, 24-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Thorsten Adler et al. paper ("the Adler paper") entitled An Interactive Router for Analog IC Design. Adler discloses an interactive two-layer router for an analog integrated circuit. Adler does not use the term "routing indicators" to define the flags which determine routing changes. However, Adler does use tunnel polygons, wave propagation and integer bit flags to control routing layout changes. It would have been obvious to one of ordinary skill in the art at the time of applicant's

invention that Adler's methods involve the use of routing controls equivalent to Applicant's routing indicators.

Pursuant to Claim 1 which recites a method for automatically routing an integrated circuit: the Adler paper discloses an interactive, automatic router; Abstract and §1;

receiving integrated circuit layout data that defines a set of two or more integrated circuit (IC) devices to be included in the IC: §2 defines two IC objects, a source (S) and a target (T);

receiving integrated circuit connection data that specifies one or more electrical connection to be made between the IC devices: §3.1, the database contains the connection information;

determining a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second IC devices: §3.1 which disclose the integer bits 21 and 29; additionally, this section discloses the use of a flag to indicate acceptable directions;

determining from the IC connection data and the set of one or more routing indicators the routing path between the first and second integrated circuit devices: §3.3 discloses path determination;

updating the IC layout data to generate updated IC layout data that reflects the routing path between the first and second IC devices: §3.4 discloses the updating and generation of final routing path data.

Pursuant to Claim 2, wherein determining the routing path includes determining based upon the IC layout data, the integrated circuit connection data (§2.4 and §3.3), bias direction criteria, §3.4, and straying limit criteria § §3.1-3.4, the routing path between the first and second integrated circuit devices, §3.3.

Pursuant to Claim 3, wherein determining the routing path between the first and second IC includes identifying one or more obstacles that block the routing path: §3.1 discloses obstacle polygons that yields unusable space;

determining indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles: §3.4; see also § §3.1-3.3;

determining. . .the routing path between the first and second integrated circuit devices: §3.4.

Pursuant to Claim 4, which recites identifying obstacle that block the routing path: §3.1 discloses the use of obstacle polygons;

changing specified straying criteria. . .: §§2.2 and 2.2.1 discloses routing path widths;

determining. . .the routing path between the first and second integrated circuit devices: §3.4.

Pursuant to Claim 5 which recites identifying obstacle that block the routing path: §3.1 discloses the use of obstacle polygons;

determining a set of one or more layer changes to allow the routing path to avoid the one or more obstacles: §3.1 discloses two level routing and an intermediate layer that Ors together level 1 and level 2 layers;

determining based upon the IC data, the IC connection data, the set of routing indicators, and the set of one or more layer changes, the routing path between the first and second integrated circuit devices: §§3.3-3.4.

Pursuant to Claim 6, which includes the limitation of determining a set of one or more bends to be included in the routing path to avoid the one more obstacle: §2.2.1.

Pursuant to Claim 10, which recites identifying one or more obstacles that block the routing path: §3.1 discloses the use of obstacle polygons;

determining . . . the routing path between the first and second integrated circuit devices: §3.3 discloses path determination.

Pursuant to Claims 11 which includes the additional limitations of determining one or more locations to employ corner clipping to provide additional space for routing the routing path: The Adler paper teaches global and maze routing which suggests corner clipping, and includes design rule modifications and routing paths of various degree angles, §§2.2 and 2.2.1;

Pursuant to Claim 12-14, Adler discloses the additional limitations of determining one or more integrated circuit layout objects to be moved to provide additional space for routing and examining data with layout changes, etc: Adler, §§1-5.

Pursuant to Claim 15, which includes the limitation of determining routing targets: Adler, §§1-5.

Pursuant to Claims 16-20, these claim include the limitation of design rule checking of routing paths and defined attachment or bend angles that are multiples of ninety degrees: Adler, Figs. 1, 2; §§2.1-2.2.2; Abstract.

Pursuant to Claim 22, which includes the limitation of determining. . .a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths: Adler, §§ 2.2 - 2.4.

Pursuant to Claims 24-28, they address the limitations previously rejected in Claims 1-5, supra and are likewise rejected using the same rationale. Claims 24-28 include the additional limitation of a computer-readable medium having instructions for automatically routing a circuit which is executed by one or more processors. The Adler paper discloses that its method is performed on a Mentor

Graphics' ICstation and its algorithms are implemented using the programming language C++. The Adler paper does not specifically disclose a computer-readable medium but it would have been obvious to one of ordinary skill in the art at the time of applicant's invention that the use of an ICstation would also include the use of computer-readable media as part of the process of implementation. See Adler, §4. Because the Adler paper also addresses the computer-readable media limitation, Claims 24-28 are unpatentable over the Adler paper.

Pursuant to Claims 29-33, they address the limitations previously rejected in Claims 1-5, supra and are likewise rejected using the same rationale. Claims 29-33 include the additional limitation of a system for automatically routing an integrated circuit. This limitation is also addressed by the Adler paper's disclosure of the Mentor Graphics' ICstation.

Pursuant to Claim 34, wherein each routing indicator from the set of one or more routing indicators specifies a routing direction for the routing path: §3.1 discloses an integer value wherein bits 21 to 29 store information about routing direction and bits 31 and 30 are used to mark grid points inside source or target polygons.

allowable subject matter

Rejection of Claims 7-9

9. **Claims 7 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Adler paper as applied to Claim 1 above and further in view of the Tzeng et al. paper ("the Tzeng paper")

entitled Codar: A Congestion-Directed General Area Router. The Adler paper discloses an interactive router for Analog IC Design. Although a rip-up and reroute algorithm may be considered part of Adler's analog route and global route algorithm, the Adler paper does not explicitly detail its inclusion. The Tzeng paper discloses the rip up and reroute process of a global and detailed routing process. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify and integrate the teaching of the Adler paper with the Tzeng paper for a more effective and efficient routing process.

Pursuant to Claims 7 and 9, Tzeng discloses the additional limitation of determining one or more portions of one or more routing paths to be ripped up and rerouted: Tzeng, §§1-5.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Adler paper in view of the Tzeng paper as applied to Claim 7, supra, and further in view of the Tzeng paper. Tzeng also suggests the limitation of determining one or more portions of one or more other routing paths to be ripped up and rerouted: Tzeng, §§1-5.

Rejection of Claim 21

10. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over the Suzuki et al. paper ("the Suzuki paper") entitled A Practical Online Design Rule Checking System. The Suzuki paper discloses a method for verifying an IC layout using a design rule checking system. The Suzuki paper's incremental DRC method does not restrict the number of design rule checks to two.

However, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention that because the Suzuki paper's incremental DRC method includes the possibility of one or more DRC's, applicant's "second design rule check" limitation is within the scope of the Suzuki paper. Pursuant to Claim 21, Suzuki discloses an automatic, incremental and iterative (to enable a second design rule check) design rule check system, §§2-3.2.

Rejection of Claim 23

11. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Xiong, U.S. patent 5,550,748. Xiong discloses a system and method for delay routing and signal net matching. Xiong does not explicitly teach the step of updating the IC layout data after changes are made. However, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention that the process of routing and rerouting as disclosed by Xiong would necessarily include updating the IC layout. Pursuant to Claim 23, the limitations of this claims are addressed by Xiong, Figs. 3, 4; Xiong, col. 2, line 44 to col. 3, line 13.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782 or the Customer Service Center whose telephone number is (703)306-5631.

13. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 305-3431, (for formal communications intended for entry)

(for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
FEBRUARY 7, 2001

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